Basics of Operational Amplifiers and Comparators

Outline:

This application note describes the basics and the terminology of operational amplifiers and comparators. We hope you will find it informative and helpful regarding your use of operational amplifiers and comparators.

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1. Introduction

Operational amplifiers (op-amps) are used not only to perform mathematical operations but also as voltage amplifiers in the most basic configuration and as filters, phase shifters, and buffers. Op-amps are widely used for various applications. It is no exaggeration to say that op-amps are found in almost all electrical appliances. For example, op-amps amplify analog signals from various sensors in IoT-connected home appliances and measuring instruments.

Voltage comparators are one of the applications of op-amps. Op-amp voltage comparators compare a signal's voltage with a reference voltage and output a signal that indicates which is larger.

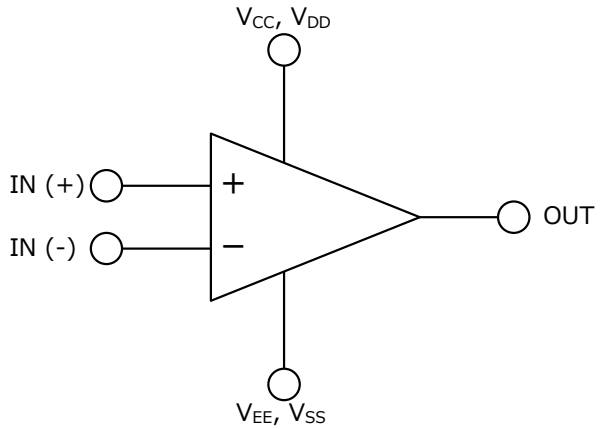
This application note describes the basic functions, usage, electrical characteristics, and terminology of op-amps and comparators. It includes somewhat technical descriptions using mathematical equations and graphs. You can skip these descriptions if you only want to know how to use op-amps and comparators.

Basically, this application note describes op-amps and comparators with dual (positive and negative) power supplies unless otherwise noted. Simply replace V_{EE} (V_{SS}) with GND, GND with the midpoint voltage between GND and V_{CC} (V_{DD}), if you are interested in op-amps and comparators with a single power supply.

2. Op-amps and comparators

2.1. Op-amp and comparator configurations

Fig.2.1.1 shows the electronic symbol for op-amps and comparators.



V_{CC}, V_{DD}: Positive power supply
V_{EE}, V_{SS}: Negative power supply
IN (+): Noninverting input
IN (-): Inverting input
OUT: Output

Fig.2.1.1 Circuit diagram symbol for op-amps and comparators

An op-amp has five terminals: positive power supply, negative power supply, noninverting input, inverting input, and output. Generally, these terminals are named as shown above. In a dual-supply configuration, a positive voltage is applied to the V_{CC} (V_{DD}) terminal and a negative voltage is applied to the V_{EE} (V_{SS}) terminal. In a single-supply configuration, the V_{EE} (V_{SS}) terminal is connected to GND. The power supply terminals are generally named V_{CC} and V_{EE} for bipolar devices whereas they are named V_{DD} and V_{SS} for CMOS devices.

Since an op-amp is a differential amplifier, it amplifies a difference in voltage between the noninverting and inverting inputs and produces a single output voltage. The polarity of the output signal is the same as that of the noninverting input and opposite to that of the inverting input. Therefore, if the same signal is applied to both the noninverting and inverting inputs, ideally no signal appears at the output.

An ideal op-amp has infinite input impedance and zero output impedance. Although real op-amps exhibit neither infinite input impedance nor zero output impedance, they are designed to provide high input impedance and low output impedance. Generally, CMOS op-amps have higher input impedance than bipolar op-amps. However, in most cases, the input and output impedances are not a concern for bipolar op-amps.

Fig.2.1.2 shows an equivalent circuit of an op-amp that models input and output impedances.

In Fig.2.1.2, V_{i+} and V_{i-} are the input voltage sources, V_O is the output signal voltage, V_+ is the voltage at the noninverting input terminal, and V_- is the voltage at the inverting input terminal. R_S represents the impedance (resistance) of the input signal sources, and R_L represents the load resistance.

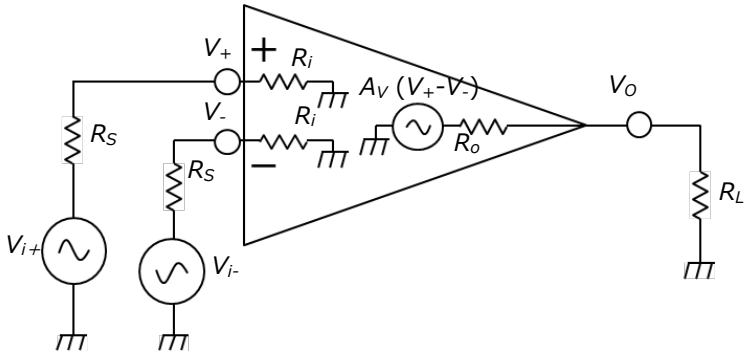


Fig.2.1.2 Equivalent circuit of an op-amp that models input and output impedances

As described above, an op-amp amplifies a difference in voltage between the noninverting and inverting inputs. Therefore, the output signal voltage (V_O) is expressed as follows:

$$V_o = \frac{R_L}{R_o+R_L} \times A_V \times (V_+ - V_-) = \frac{R_L}{R_o+R_L} \times A_V \times \frac{R_i}{R_i+R_S} \times (V_{i+} - V_{i-}) \quad \ldots (2.1.1)$$

Where R_i, R_O, and A_V are the characteristics of an op-amp. R_i is the input impedance, R_O is the output impedance, and A_V is the open-loop gain (i.e., the ratio of output voltage to input voltage). If the input impedance (R_i) is sufficiently high and the output impedance (R_O) is sufficiently low, the two terms that represent their ratio in Equation 2.1.1 are close to 1. In this case, this equation is approximated as follows:

$$V_o = A_V \times (V_{i+} - V_{i-}) \quad \ldots (2.1.2)$$

Real op-amps are designed to provide high input impedance and low output impedance so as to make this approximation possible.

2.2. Selecting op-amps and comparators

Op-amps and comparators are divided into CMOS and bipolar devices according to the type of internal elements.

CMOS op-amps and comparators consist of only complementary metal-oxide-semiconductor (CMOS) transistors whereas bipolar op-amps and comparators consist of only bipolar transistors.

Table 2.2.1 compares the characteristics of CMOS and bipolar devices. Double circles indicate the characteristics generally desired for op-amps and comparators, but the absence of a double circle does not mean that either type is unsuitable.

Table 2.2.1 Comparison of CMOS and bipolar op-amps and comparators

	CMOS	Bipolar
Input impedance	◎ High	Lower than CMOS devices
Input offset voltage	Large variations	◎ Small variations
Input bias current	◎ Low (Bias current does not flow to the gate because of the MOS structure.)	High (Base current is used as a bias source.)
Maximum output voltage swing	◎ High (for full-swing outputs)	Low
Power dissipation (heat dissipation)	◎ Low	High
Breakdown voltage	Low	◎ High
Operating speed	Low	◎ High
Noise	Higher than bipolar devices ◎ (Low in the case of low-noise devices)	◎ Low

It is generally said that bipolar op-amps and comparators should be used for applications requiring low noise whereas CMOS op-amps and comparators should be used for applications requiring high input impedance such as analog sensors. It is difficult, however, to generalize in this way because low-noise CMOS op-amps and comparators are appearing.

Both CMOS and bipolar devices have advantages and disadvantages. Consider input signal levels, frequency bands, power supply conditions, intended use, and objectives to determine your priorities and which type of device satisfies them.

2.3. Power supplies for op-amps and comparators

One of the key points in selecting op-amps and comparators is whether they are powered from single or dual power supplies. Op-amps and comparators are available in types intended for use in

single- and dual-supply configurations.
In brief, if the data sheet of an op-amp or a comparator shows the maximum rated supply voltage as ±X (V), it is designed for use with dual power supplies. An op-amp or a comparator with only a positive maximum supply voltage specification is designed for use with a single power supply.
In the early days, op-amps were used with dual power supplies. However, as electronic devices that operate with a single power supply become increasingly common, those designed for use with a single power supply have appeared. Some op-amps for single-supply applications are capable of full-swing input and output signaling. The input circuit of these op-amps is designed to allow the input signal to swing to the GND potential.
It is possible to operate op-amps for dual-supply applications with a single power supply or operate op-amps for single-supply applications with dual power supplies, but in such cases, care should be taken as to the maximum rated supply voltage and common-mode input voltage.
See Section 3.3 for common-mode input voltage. See Section 4.1 for the maximum rated supply voltage.

2.4. Noninverting amplifier

In the most basic form, op-amps are used as voltage amplifiers. This section describes the use of an op-amp as a voltage amplifier.
Fig.2.4.1 shows an example of a noninverting amplifier with a closed loop and its gain. Both R_1 and R_2 are external resistors. In this circuit, negative feedback is used to apply a portion of the output voltage to the inverting input via R_1 and R_2. The closed-loop gain (G_V) of this circuit is expressed only with R_1 and R_2. The ease of gain setting is one of the advantages of an op-amp.
Hereinafter, A_V and G_V represent the open- and closed-loop gains respectively.
Reducing the values of external feedback resistors helps reduce the effect of input bias current (see Section 3.2), but the load resistance and the op-amp's output current capability should be taken into consideration when selecting the optimum feedback resistors.

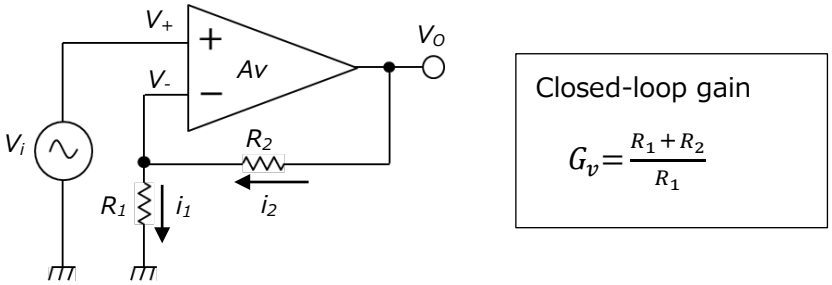


Fig.2.4.1 Noninverting amplifier

The closed-loop gain of this circuit can be calculated as follows.
An ideal op-amp has the following relationships between voltage and current:

$$V_o = A_V(V_+ - V_-)$$
$$i_1 = \frac{V_-}{R_1}$$
$$i_2 = \frac{V_o - V_-}{R_2}$$

Because the input impedance is infinite, $V_+ = V_i$ and $i_1 = i_2$. Hence, the closed-loop gain (G_V) of this noninverting amplifier can be calculated as follows:

$$G_v = \frac{V_o}{V_i} = \frac{R_1 + R_2}{(1+A_v)R_1 + R_2} A_v \quad \ldots (2.4.1)$$

If A_V is sufficiently greater than 1, G_V can be approximated as follows by dividing the numerator and denominator of the right-hand side of the equation by $1 + A_V$:

$$G_v = \frac{V_o}{V_i} \cong \frac{R_1 + R_2}{R_1} \quad \left(\frac{A_V}{1+A_V} \cong 1,\ \frac{1}{1+A_V} \cong 0\right) \ldots (2.4.2)$$

For this approximation, the op-amp needs to have a sufficiently high open-loop gain (A_V). Since op-amps are typically designed to exhibit an open-loop gain on the order of 10^5 (100 dB), the closed-loop gain (G_V) can be determined by external resistors in most cases.
Negative feedback reduces the output voltage swing of the op-amp, reducing the difference in voltage between the noninverting and inverting inputs to nearly zero. This is called a virtual short circuit (or simply a virtual short), which is one of the important considerations in creating application circuits of an op-amp.
The following paragraphs describe a voltage follower circuit, one of the simplest forms of a noninverting amplifier with a virtual short.
Fig.2.4.2 shows a voltage follower and its closed-loop gain.

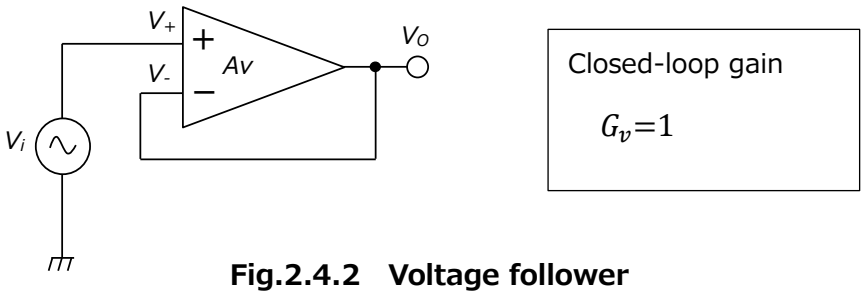


Fig.2.4.2 Voltage follower

In the voltage follower, R_1 is infinite and R_2 is equal to zero. As a result, all of the output voltage is applied to the inverting input.

Because V_+ and V_- are virtually shorted, the output voltage is almost equal to the input voltage. A voltage follower is commonly used as a buffer since it provides impedance conversion from a high to a low level. Its closed-loop gain (G_V) is calculated as follows.

From Fig.2.4.2, $V_+ = V_i$ and $V_- = V_o$. Hence, from the equations shown in the description of the noninverting amplifier:

$$V_o = A_V(V_+ - V_-) = A_V(V_i - V_o)$$

This equation can be restated as:

$$\frac{V_o}{A_V} = V_i - V_o$$

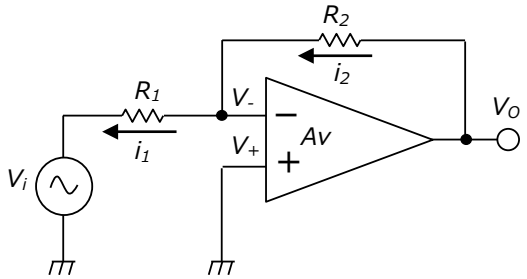
Since A_V is sufficiently higher as described above, the left-hand side of this equation can be approximated to zero. Thus, the voltage gain (G_V) is calculated as follows:

$$V_i \cong V_o$$
$$G_v = \frac{V_o}{V_i} \cong 1 \quad \text{... (2.4.3)}$$

Also see Section 3.6, "Maximum output voltage swing," and Section 3.12, "Oscillation immunity," when using a voltage follower.

2.5. Inverting amplifier

Fig.2.5.1 shows an inverting amplifier and its closed-loop gain.



Closed-loop gain

$$G_v = -\frac{R_2}{R_1}$$

Fig.2.5.1 Inverting amplifier

R_1 and R_2 are external resistors. As is the case with a noninverting amplifier, an inverting amplifier uses negative feedback. Therefore, the closed-loop gain of the inverting amplifier can be calculated with a simple equation shown in Fig.2.5.1. This equation can be obtained as follows.

An ideal op-amp has the following relationships between voltage and current:

$$V_o = A_V(V_+ - V_-)$$
$$i_1 = \frac{V_- - V_i}{R_1}$$
$$i_2 = \frac{V_o - V_-}{R_2}$$

Because the input impedance is infinite, $V_+ = 0$ and $i_1 = i_2$. Hence, the closed-loop gain (G_V) of this inverting amplifier can be calculated as follows:

$$G_v = \frac{V_o}{V_i} = -\frac{R_2}{(1+A_v)R_1+R_2}A_v \ldots (2.5.1)$$

If A_V is sufficiently greater than 1, G_V can be approximated as follows, as is the case with a noninverting amplifier:

$$G_v = \frac{V_o}{V_i} \cong -\frac{R_2}{R_1} \quad \left(\frac{A_V}{1+A_V} \cong 1,\ \frac{1}{1+A_V} \cong 0\right) \ldots (2.5.2)$$

The right-hand side of the equation has a negative sign, indicating that the input and output signals have the opposite phase.
As is the case with a noninverting amplifier, the values of external feedback resistors should be minimized, taking the load resistance and the op-amp's output current capability into consideration.
The inverting amplifier also has a virtual short between the noninverting and inverting inputs.

2.6. Basics of comparators

Like an op-amp, a comparator has five terminals: positive power supply, negative power supply, noninverting input, inverting input, and output.
Comparators do not have feedback except for special cases. One of the inputs is connected to a fixed reference voltage, and the voltage to be monitored is applied to the other input. Then, the output indicates whether it is higher or lower than the reference voltage.
A comparator acts as follows when the inverting input is connected to a reference voltage and the voltage to be monitored is connected to the noninverting input:

Voltage to be monitored (noninverting input) < reference voltage (inverting voltage)
→ The output terminal provides a Low level.
Voltage to be monitored (noninverting input) > reference voltage (inverting voltage)
→ The output terminal provides a High level.

Alternatively, the noninverting input can be used as a reference voltage input. In that case, the comparator acts as follows:

Voltage to be monitored (inverting input) < reference voltage (noninverting voltage)
→ The output terminal provides a High level.
Voltage to be monitored (inverting input) > reference voltage (noninverting voltage)
→ The output terminal provides a Low level.

Fig.2.6.1 shows a comparator using the inverting input as a reference voltage input and its

operation. V_{ref} is the reference voltage. Determine which input to use as a reference voltage according to the configuration of the circuit following the comparator output.

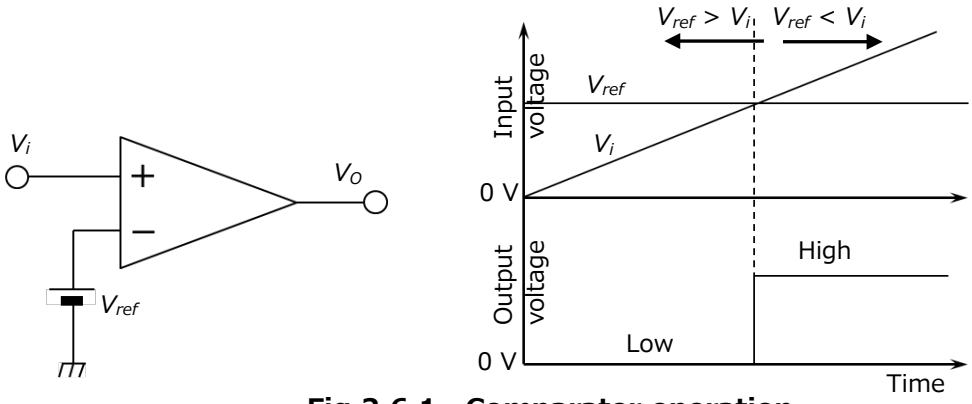


Fig.2.6.1 Comparator operation

Comparators are available with either an open-collector (or an open-drain for CMOS) or push-pull output (see Section 3.6).

The open-collector (open-drain) output consists of a single transistor, which either sinks or sources output current. An open-collector (open-drain) comparator requires either a pull-up resistor between the output terminal and V_{CC} (V_{DD}) or a pull-down resistor between the output terminal and V_{EE} (V_{SS}). Which resistor is required depends on the polarity of the output transistor.

In contrast, the push-pull output consists of two stacked transistors, which can both sink and source the output current. A push-pull comparator requires neither a pull-up nor a pull-down resistor.

See the data sheet of each comparator for its output configuration.

The following consideration applies when using a device sold as an op-amp to form a comparator. Op-amps are designed for use with negative feedback. Typically, op-amps incorporate a phase compensation capacitor to prevent feedback oscillation (see Section 3.12). The phase compensation capacitor causes an increase in output response times. Ensure that this increase does not pose any problem. In contrast, devices sold as comparators do not incorporate a phase compensation capacitor. You can use them as comparators without any such concern. See Section 3.14 for response times.

All op-amps have a push-pull output. It should be noted that the Low and High levels might not be equal to the GND and V_{CC} (V_{DD}) voltages. The output voltage swing might be roughly 1 V lower than the supply voltage range. This is detailed in Section 3.6, “Maximum output voltage swing.”

3. Basic electrical characteristics

This section describes major electrical characteristics shown in the data sheets of op-amps and comparators as well as other characteristics that are important in creating application circuits.

3.1. Input offset voltage

Input offset voltage is defined as a difference in voltage that occurs between the two input terminals of an op-amp or a comparator. Select op-amps and comparators with minimal input offset voltage.

An ideal op-amp has an input offset voltage of zero, which means that the noninverting input voltage is exactly equal to the inverting input voltage. In reality, however, a small current flows through the input terminals because the input impedance is not infinite. In addition, because of manufacturing process variations, the internal elements that constitute the differential amplifier circuit of a real op-amp might not be exactly matched. Piezoelectric effects also occur owing to changes in stress caused by bent mold resin or substrate. The effects of these factors are not negligible. These factors cause a difference in voltage between the two input terminals called input offset voltage.

An op-amp amplifies the input offset voltage, causing the output voltage to drift from 0 V.

Fig.3.1.1 shows the waveform of the voltage that appears at the output of a noninverting amplifier when there is input offset voltage (V_{IO}).

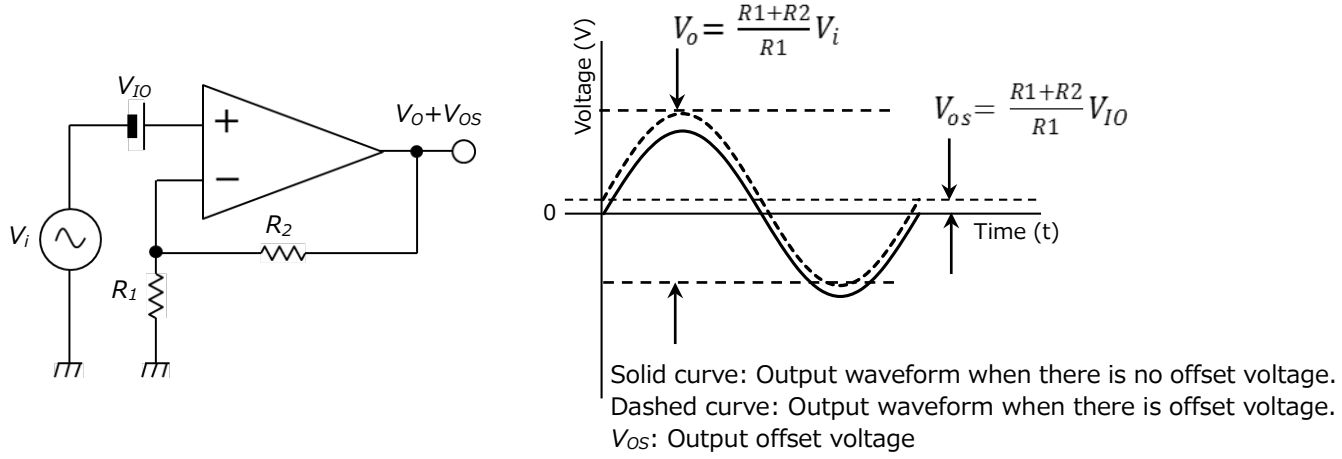


Fig.3.1.1 Output waveform of a noninverting amplifier when there is input offset voltage

As described above, the input offset voltage of an op-amp causes an offset of output voltage. This causes an error in applications in which the output voltage from a sensor is detected via DC voltage or an analog signal is converted into a digital signal with an AD converter.

In the case of a comparator, the input offset voltage results in a detection error since it is added to or subtracted from the voltage to be monitored. An error in the output voltage also causes a target voltage to be detected earlier or later than it should be detected.

Generally, input offset voltage varies with temperature. This is called a temperature drift, which is shown in the data sheets of some op-amps. Care should also be exercised as to the temperature drift.

3.2. Input bias current and input offset current

Input bias current is the current that flows into the input terminals of an op-amp described above. As is the case with input offset voltage, input bias current should also be minimal. It is important to select op-amps with minimal input bias current.

In a bipolar op-amp, the base current of the transistor pair connected to the input terminals and the leakage current that flows from the input terminals to GND contribute to the input bias current. The base current is the major contributor to the input bias current since it is generally larger than the leakage current. If the differential input circuit consists of a PNP transistor pair, input bias current flows out of an op-amp. If the differential input circuit consists of an NPN transistor pair, input bias current flows into an op-amp.

In the case of a CMOS op-amp, only the leakage current from the input terminals contributes to input bias current because no base current flows in the CMOS op-amp. Therefore, CMOS op-amps exhibit much lower input bias current than bipolar op-amps and should be selected for applications requiring high accuracy such as sensors.

If the internal transistors at the noninverting and inverting inputs have symmetrical electrical characteristics, the offset voltage generated by input bias current can be canceled out by inserting R_3 that is equal to the equivalent resistance of parallel R_1 and R_2. Fig.3.2.1 shows a noninverting amplifier with a bias current cancellation resistor.

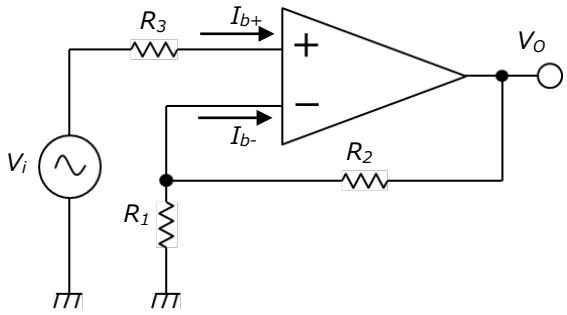


Fig.3.2.1 Noninverting amplifier with a bias current cancellation resistor

In Fig.3.2.1, I_{b+} is the bias current flowing into the noninverting input terminal, I_{b-} is the bias current flowing into the inverting input terminal, and R_3 is a bias current cancellation resistor. V_O can be calculated as follows in the same manner as described in the previous section:

$$V_o = \frac{R_1+R_2}{R_1} V_i + \underbrace{\frac{R_1+R_2}{R_1} \times R_3 \times I_{b+} - R_2 \times I_{b-}}_{\text{Output offset voltage } = V_{OS}} \quad \ldots (3.2.1)$$

The last two terms on the right-hand side of this equation represent output offset voltage, i.e., an error in the output voltage, caused by input bias current. Therefore, the conditions that reduce the result of these two terms to zero should be considered.

$$\frac{R_1+R_2}{R_1} \times R_3 \times I_{b+} - R_2 \times I_{b-} = 0 \quad \ldots (3.2.2)$$

Making R_3 the subject of the equation gives:

$$R_3 = \frac{R_1 R_2}{R_1 + R_2} \times \frac{I_{b-}}{I_{b+}} \quad \text{... (3.2.3)}$$

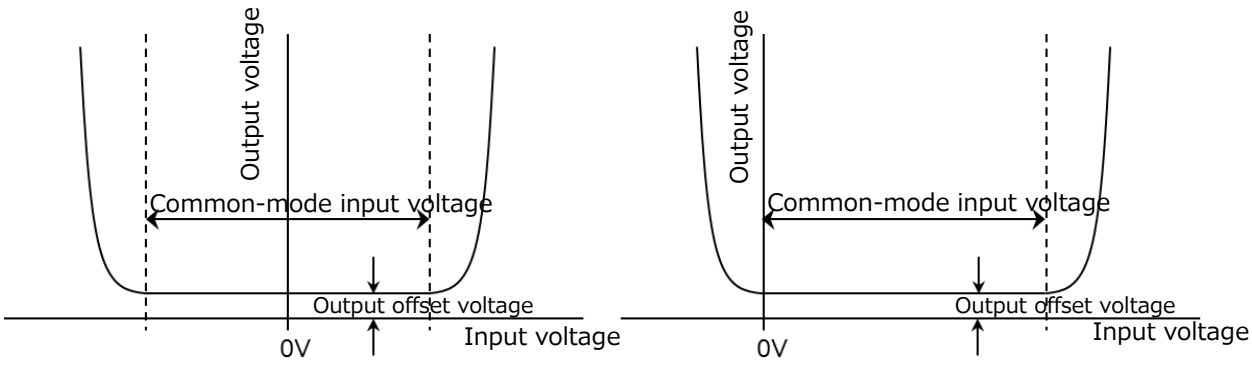
If the differential input transistor pair is completely symmetrical, I_{b+} is equal to I_{b-}. Then, Equation 3.2.3 is simplified to:

$$R_3 = \frac{R_1 R_2}{R_1 + R_2} \quad \text{... (3.2.4)}$$

This is equal to the equivalent resistance of parallel R_1 and R_2. Therefore, inserting R_3 equal to this value reduces the output offset voltage to zero (i.e., the result of Equation 3.2.2 becomes zero).
The differential input circuits of op-amps are carefully designed in terms of symmetry. However, the bias currents flowing to the noninverting and inverting inputs might not be matched because of manufacturing variations. The difference in input bias current between the noninverting and inverting input terminals is called input offset current.
Equation 3.2.2 indicates that input offset current results in output offset voltage, which cannot be canceled out.

3.3. Common-mode input voltage

Common-mode input voltage is defined as a range of voltage that can be applied to an op-amp. If a voltage exceeding common-mode input voltage is applied, large offset voltage appears at the output, causing the op-amp not to operate properly. Typically, an equal DC voltage is applied to the noninverting and inverting inputs of an op-amp. Then, the op-amp amplifier provides an amplified voltage around the input DC voltage. This DC voltage is called input bias voltage. It is necessary to set the input bias voltage to a value within the common-mode input voltage range, taking the input signal swings into consideration.
The common-mode input voltage is determined by the configuration of the differential input circuit in an op-amp. See the data sheet of each op-amp for common-mode input voltage.
Some op-amps designed for use with a single power supply allow a voltage as low as the GND potential to be applied to the negative input. The data sheets of these op-amps show the lower limit of the common-mode input voltage as 0 V. Select op-amps suitable for your applications, considering electrical characteristics and their test conditions.
Fig.3.3.1 illustrates the common-mode input voltage of op-amps for dual- and single-supply applications.



a) Dual power supplies b) Single power supply

Fig.3.3.1 Common-mode input voltage

Most dual-supply op-amps can be used with a single power supply by setting the input bias voltage to the neutral point voltage (i.e., one-half of the supply voltage). In this case, care should be taken as to common-mode input voltage.

3.4. Supply current

Supply current is the current that flows from the positive power supply terminal (V_{CC}, V_{DD}) to the negative power supply terminal (V_{EE}, V_{SS}) when an op-amp has no input and thus no output signals. Supply current is dissipated as heat in the internal resistance of op-amps and comparators. The lower the supply current, the lower the heat dissipation. It is advisable to select op-amps and comparators with minimal supply current, considering a temperature drift.
Typically, CMOS devices exhibit lower supply current than bipolar devices.

3.5. Voltage gain

A voltage gain refers to the open-loop gain, i.e., the gain obtained when no feedback is used in the circuit. When negative feedback is used, a higher open-loop gain provides better AC characteristics (e.g., less noise) and less error in the closed-loop gain. However, op-amps with a higher open-loop gain apply a greater portion of the output voltage (i.e., a greater amount of feedback) to the inverting input, causing them to become more unstable and susceptible to oscillation.
As described in Section 2.4, op-amps are typically designed with an open-loop gain on the order of 10^5 (100 dB).

3.6. Maximum output voltage swing

The maximum output voltage swing is the maximum voltage swing obtained at the output of an op-amp or a comparator.

There are ranges of voltage close to V_{DD} (V_{CC}) and V_{SS} (V_{EE}) that cannot be obtained at the output terminal. These ranges are determined by the output circuit configuration. The maximum output voltage swing indicates the range of the voltage in which the output signal can swing. The greater the maximum output voltage swing, the greater the swing of the output signal.

Most CMOS devices are designed to allow the output signal to swing the full range between V_{DD} and V_{SS}. Such op-amps are called full-swing op-amps. All Toshiba's CMOS op-amps are full-swing op-amps.

The output voltage swing depends on supply voltage and load resistance. Therefore, op-amps and comparators should be selected, taking these conditions into consideration in addition to the required output voltage swing. Details are described below. This characteristic is indicated as the maximum output voltage swing, maximum and minimum output voltages, or residual voltage in data sheets. The maximum and minimum output voltages are specified for Toshiba's CMOS op-amps and dual-supply bipolar op-amps whereas the maximum output voltage swing is specified for Toshiba's bipolar single-supply op-amps.

The following paragraphs detail the maximum output voltage swing using the output circuitry of a dual-supply bipolar op-amp and its output waveform shown in Fig.3.6.1.

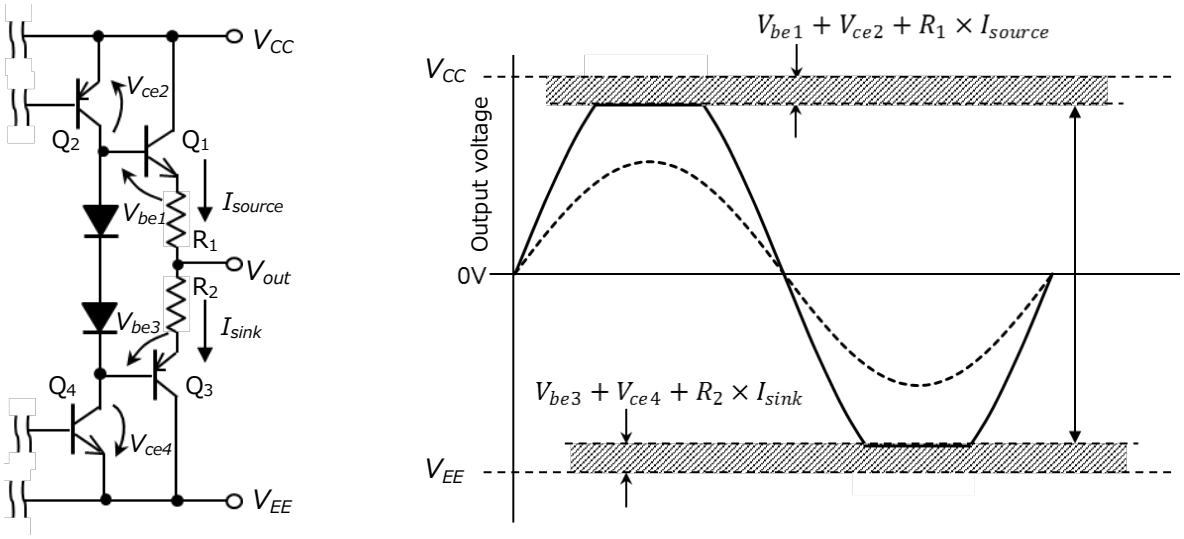


Fig.3.6.1 Output circuit commonly used in bipolar op-amps and its waveform

R_1 and R_2 connected to the emitter of Q_1 and Q_3 are current-limiting resistors to prevent their destruction.

The output consisting of two stacked transistors with opposite polarities as shown in Fig.3.6.1 is called a push-pull configuration.

In this example, when V_{out} is higher than $V_{CC} - (V_{be1} + V_{ce2} + R_1 \times I_{source})$ (i.e., when V_{out} is in the upper shaded range), Q_1 and Q_2 cannot operate, unable to swing the output voltage near the V_{CC} rail. Likewise, when V_{EE} is lower than $V_{EE} + (V_{be3} + V_{ce4} + R_2 \times I_{sink})$ (i.e., when V_{EE} is in the lower shaded range), Q_3 and Q_4 cannot operate, unable to swing the output voltage near the V_{EE} rail.

These ranges to which the output voltage cannot swing are called residual voltages. The top and bottom of the output waveform are clipped off as shown in Fig.3.6.1. In other words, the maximum output voltage swing can be considered to be the output voltage range that is not clipped.

In this example, there is residual voltage near the V_{CC} and V_{EE} rails. Some single-supply bipolar op-amps incorporate an output circuit in a different configuration so as to be able to swing the output voltage to a level close to GND when a sink current is low.

As described above, most CMOS op-amps incorporate full-swing output circuitry.

As you see from the above description, the maximum output voltage swing depends on supply voltage. In addition, the source current (I_{source}) and the sink current (I_{sink}) in the above equations include the current that is sourced from or sunk into the output terminal, which is determined by the load resistance. Therefore, the maximum output voltage swing also depends on the load resistance. Pay attention to the supply voltage and load resistance conditions when examining op-amp data sheets.

The maximum output voltage swing of an op-amp can decrease when it is used with a lower closed-loop gain than the value shown in the data sheet. This is because when the closed-loop gain is set to a low value, the input voltage swing exceeds the common-mode input voltage before the output voltage reaches the maximum output voltage swing, causing the signal to be limited at the input stage. In this case, the output voltage cannot reach the maximum output voltage swing. Care should be taken when the closed-loop gain of a voltage follower or other op-amp circuits is set to a low value.

3.7. Common-mode rejection ratio

The common-mode rejection ratio (CMRR) represents a change in the input offset signal that occurs when the same signal (common-mode input) is applied to both the noninverting and inverting inputs. A high CMRR is desirable because it means less leakage of the common-mode input signal to the output.

The CMRR is defined as a ratio of the common-mode voltage gain to the differential voltage gain. Normally, the CMRR is calculated as follows by measuring a change in the output offset voltage while changing the input DC voltage. Fig.3.7.1 shows a test circuit for the CMRR.

$$\mathrm{CMRR} = 20\log\left(\left|\frac{\Delta V_I}{\Delta V_O}\right| \times \frac{R_1}{R_1 + R_2}\right)$$

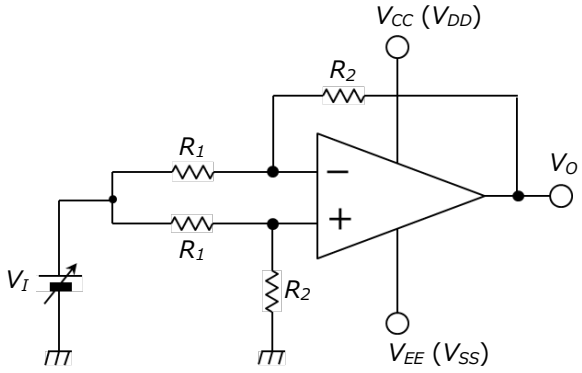


Fig.3.7.1 Test circuit for the common-mode rejection ratio

3.8. Supply voltage rejection ratio

The supply voltage rejection ratio (SVRR) represents a change in the input offset voltage that occurs in response to changes in supply voltage. It is also called the power supply rejection ratio (PSRR). A high SVRR is desirable because it means less leakage of supply voltage changes to the output.

The SVRR is defined as the ratio of the gain due to changes in supply voltage to the differential voltage gain. Normally, the SVRR is calculated as follows by measuring the output offset voltage while changing the supply voltage. Fig.3.8.1 shows a test circuit for the SVRR.

$$\mathrm{SVRR} = 20\log\left(\left|\frac{\Delta(V_{CC}-V_{EE})}{\Delta V_O}\right| \times \frac{R_1}{R_1+R_2}\right)$$

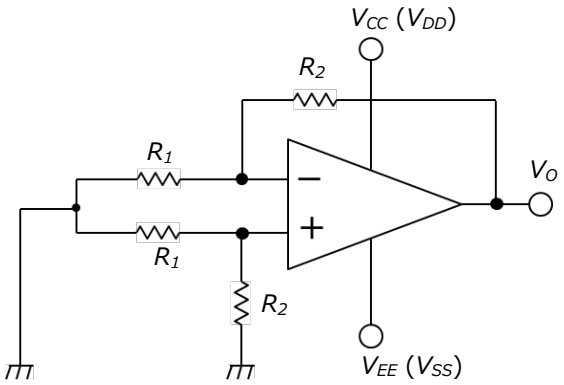


Fig.3.8.1 Test circuit for the power supply rejection ratio

3.9. Source current and sink current

Both source and sink currents indicate the current drive capability of op-amps and comparators. Source current is defined as the current flowing out of the output terminal whereas sink current is defined as the current flowing into the output terminal. When the output is at a High level, the upper transistor in the push-pull output shown in Section 3.6 provides a source current to the load resistor. When the output is at a Low level, the lower transistor draws a sink current from the load resistor. Source and sink currents might differ, depending on the output circuit configuration. Select op-amps and comparators suitable for your objective, considering the impedance of the load to be driven and the supply voltage.

Normally, the source current is measured by inserting an ammeter between the output terminal and V_{EE} at input conditions ($V_+ > V_-$) that provide a High output whereas the sink current is measured by inserting an ammeter between the output terminal and V_{CC} at input conditions ($V_+ < V_-$) that provide a Low output. Since the internal impedance of an ammeter is very small, the measured source and sink currents represent the maximum currents that can flow out of or into the output transistors.

Some comparators consist of a single transistor in an open-collector configuration (or an open-drain configuration for CMOS comparators) as described in Section 2.6. For such comparators,

either the source current or the sink current is specified in data sheets, depending on the polarity of the output transistor.

3.10. Slew rate

The slew rate (SR) is a metric used to indicate the speed of a low-to-high or high-to-low transition of the output of an op-amp.

Generally, the slew rate is defined as a ratio of the time required for the output to change from 10% to 90% or from 90% to 10% of its maximum value to a change in voltage when a high-swing square-wave input is applied. To put it simply, the slew rate is an increase or decrease in voltage that can occur in 1 μs. The smaller value of the low-to-high or high-to-low slew rates is shown in data sheets.

Fig.3.10.1 shows the slew rate of the output waveform that appears in response to an input waveform.

When the slew rate is considered as the slope of the tangent (i.e., differential value) at the zero-crossing point of a sinusoidal wave (the midpoint of a voltage swing), it represents the frequency of a signal that an op-amp can amplify while maintaining a certain swing. Calculate the operating speed from the maximum frequency at which an op-amp will be used and the output swing required at that frequency, and select an op-amp with a higher slew rate than this result.

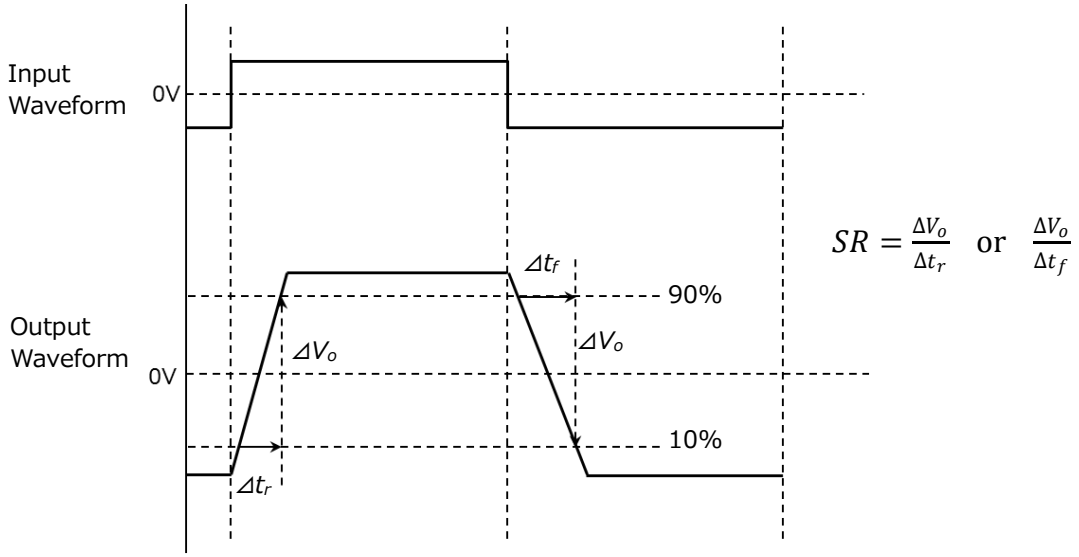


Fig.3.10.1 Slew rate (SR)

3.11. Frequency characteristics

For op-amps, the open-loop gain-vs-frequency and phase-vs-frequency characteristics are important.

In real op-amps, a low-pass filter is formed at the output by the output impedance and the terminal and load capacitances. Therefore, as the input frequency increases, the open-loop gain decreases. In data sheets, the frequency at which the open-loop gain becomes 0 dB is specified as the unity gain cross frequency.

The phase of the output signal lags behind that of the input signal as the open-loop gain decreases. At a certain frequency, the gain begins to decrease at a slope of -6 dB/oct (-20 dB/dec). This frequency is called a pole.

The phase begins to lag behind at one-tenth of the first pole frequency. The phase lag becomes 45° at the first pole frequency and levels off at 90° at ten times the first pole frequency. As the frequency increases further, the gain decreases further at a slope of -6 dB/oct, reaching -12 dB/oct at the second pole frequency. The phase lag also increases by another 45°, reaching 135° at the second pole frequency and reaches 180° at ten times the second pole frequency.

A combination of two logarithmic plots, expressing the magnitude in decibels (dB) of frequency response of the gain and the phase shift, is called a Bode plot. Fig.3.11.1 shows an example of a Bode plot of an open-loop op-amp. In this Bode plot, the first pole occurs at 10 Hz, followed by the second pole at 1 MHz.

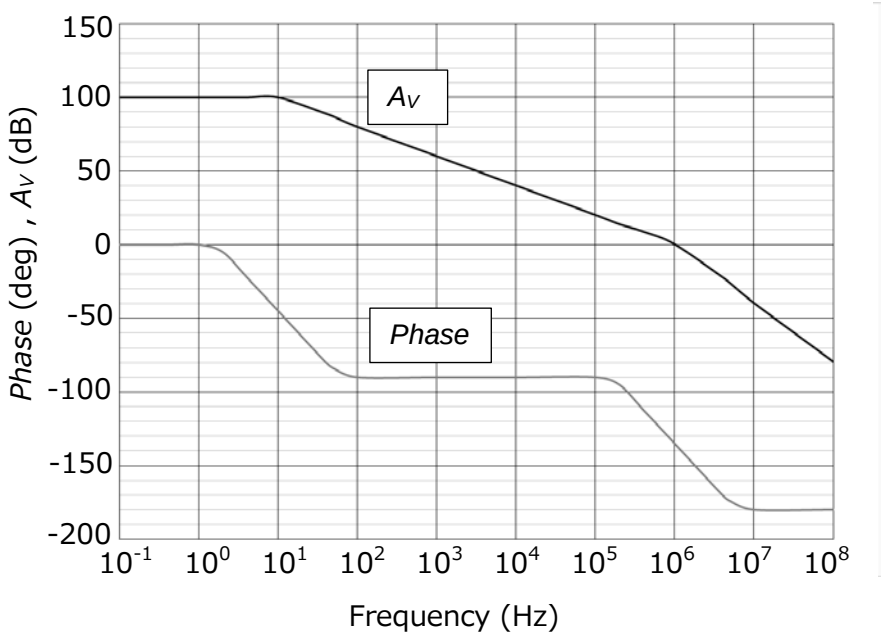


Fig.3.11.1 Example of a Bode plot of an op-amp

3.12. Oscillation immunity

It is necessary to consider the immunity to oscillation when forming a noninverting or inverting amplifier with an op-amp. Although devices sold as op-amps incorporate a phase compensation capacitor to prevent oscillation due to output impedance and terminal capacitance, they might go into oscillation, depending on load conditions. In the event of an oscillation, it is necessary to add external capacitors and resistors to the output to suppress oscillation. Perform an on-board evaluation carefully to ensure immunity to oscillation. An op-amp with a loop that applies a greater portion of the output voltage to the input is more susceptible to oscillation. In the case of voltage followers and op-amps with a low gain, care should be taken as to oscillation.

Devices sold as comparators are not designed to prevent oscillation, as mentioned in Section 2.6. Do not use comparators with a feedback loop except for hysteresis comparators.

When an op-amp is used with a feedback loop to create an amplifier, the closed-loop gain is set to a value lower than the open-loop gain for both noninverting and inverting amplifiers. As the frequency increase, the open-loop gain decreases, as described in Section 3.11. If the open-loop gain drops below the closed-loop gain, the closed-loop gain also decreases in line with the open-loop gain at higher frequencies.

An op-amp with negative feedback means that a portion of the output voltage is applied to the inverting input. The portion of the output voltage applied to the inverting input is called the amount of feedback. The ratio of the signal applied to the inverting input via a feedback loop to the input signal is called the loop gain, which is equal to the open-loop gain multiplied by the amount of feedback. (Since amplifiers with a feedback loop have a virtual short between the noninverting and inverting inputs, their loop gain cannot be measured.) In a Bode plot, a difference between open-loop and closed-loop gains represents a loop gain. Therefore, the loop gain is 1 (i.e., 0 dB) when open-loop and closed-loop gains are equal.

A signal with a phase delay of 180° is in the opposite polarity to the input signal. Applying a signal with a phase delay of 180° to the inverting input via a feedback loop is equivalent to applying signals with the same phase to the noninverting and inverting inputs.

In this case, if the loop gain is greater than 0 dB, a feedback signal is added to the inverting input, amplified, and then applied to the inverting input again. This is equivalent to using positive feedback, causing an op-amp to become unstable and go into oscillation.

In other words, oscillation does not occur if the phase delay is less than 180° when the loop gain is 0 dB or if the loop gain is equal to or less than 0 dB when the phase delay is 180°. A difference of 180° and the phase delay that provides a loop gain of 0 dB is called a phase margin whereas the loop gain at a frequency at which the phase delay is 180° is called a gain margin.

Oscillation immunity can be determined by reading the phase and gain margins from the Bode plot shown in Section 3.11. Fig.3.12.1 shows an example of a Bode plot for a feedback amplifier and its phase and gain margins. In the case of a noninverting amplifier, a phase delay starts at 0° in a Bode plot. In the case of an inverting amplifier, the two input signals are opposite (i.e., have a phase difference of 180°) at first; therefore, a feedback signal is considered to have lagged by 180° when it has a phase delay of 0° relative to the inverting input.

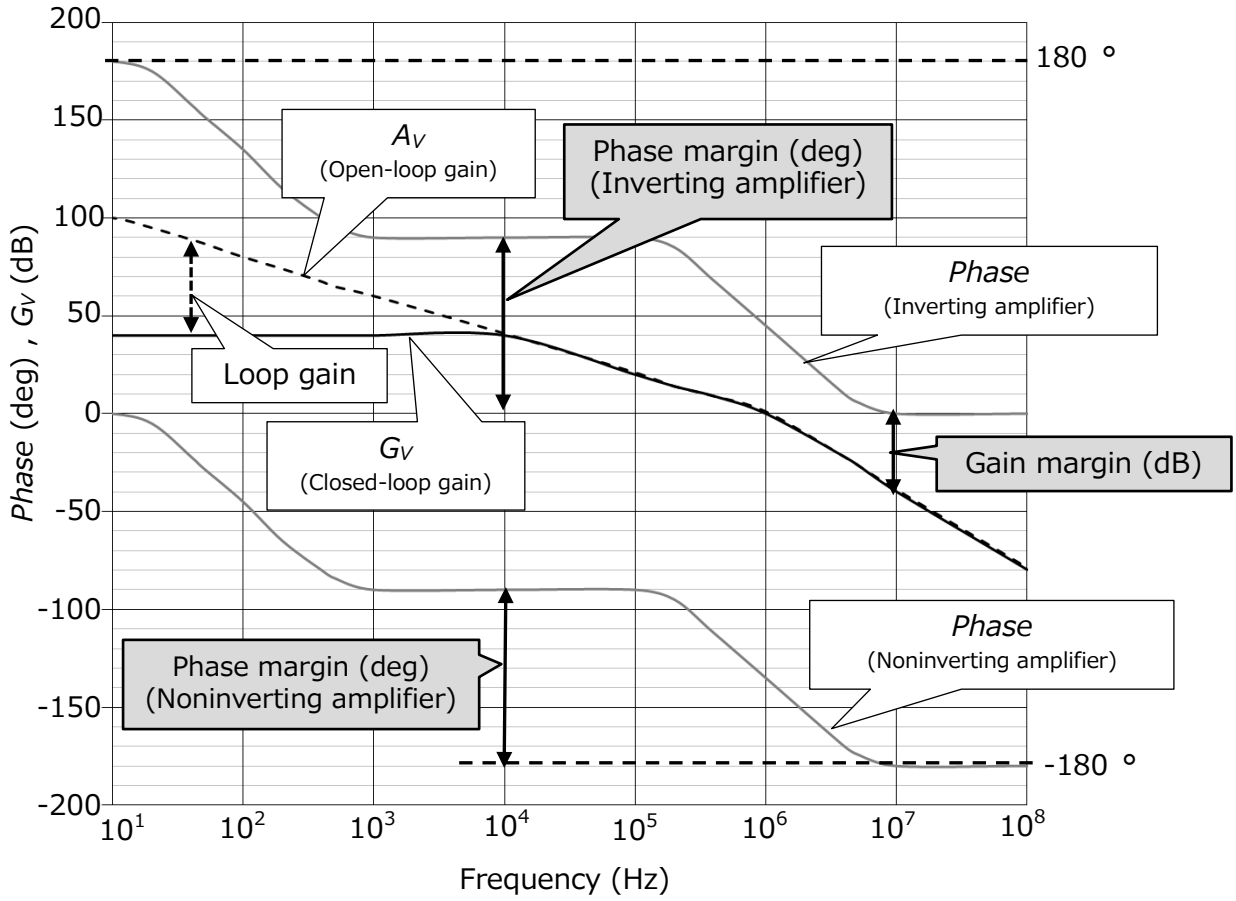


Fig.3.12.1 Gain margin and phase margin

In this example, the gain margin is roughly 40 dB, and the phase margin is 90° for both noninverting and inverting amplifiers. The amplifier has a 90° margin because the phase delay is less than 180° at a gain of 0 dB, or the gain is less than 0 dB when there is a phase delay of 180°. Therefore, the amplifier does not go into oscillation.

For more details on oscillation → Click Here

Although this application note describes the oscillation of low-dropout (LDO) regulators, its description also fully applies to op-amps.

3.13. Noise voltage

Noise voltage indicates the magnitude of noise that appears at the output of an op-amp. Generally, the output noise voltage of an op-amp divided by its gain is regarded as equivalent input noise voltage. Op-amps with minimal equivalent input noise voltage should be selected. The equivalent input noise voltage is crucial particularly for small-signal sensors. Use low-noise op-amps for these applications.

In the case of op-amp-based amplifiers, not only the noise generated inside an op-amp but also the noise generated by external components appears at its output. To reduce the output noise voltage, care should be exercised as to the selection of external components. For example, input resistors with a minimal value and low-noise capacitors should be used. In addition, the external noise

introduced via power supply or GND might affect the operation of an op-amp-based amplifier. It might be necessary to run traces around a board, modify the width of traces, and insert choke coils. There are different types of noise such as thermal noise, 1/f noise, and shot noise, which are described below.

- Thermal noise

Thermal noise is generated by the random thermal motion (Brownian motion) of free electrons inside a resistor. Thermal noise can be calculated as follows:

$$V_{nT} = \sqrt{4kTR\Delta f}$$

V_{nT}: Thermal noise voltage, k: Boltzmann constant (=1.38×10^{-23}), T: Absolute temperature, R: Resistance value

Δf: Noise bandwidth

This equation indicates that thermal noise depends on resistance and temperature. Thermal noise is white noise, meaning that its frequency spectrums spread across a wide range.

- 1/f noise (flicker noise)

Although controversy exists as to the mechanism of flicker noise, it is generally considered to be generated by the catch-and-release of carriers by missing bonds on semiconductor interfaces. Flicker noise is pink noise, meaning that its spectrum is inversely proportional to the frequency.

- Shot noise

Shot noise results from statistical fluctuations of an electric current in a semiconductor caused by random motion of charge carriers (electrons or holes). Shot noise is white noise whose frequency spectrum spreads across a wide range.

- Current distribution noise

Current distribution noise is a slight disturbance generated when a current is distributed.

- Burst noise

Burst noise consists of sudden step-like transitions between discrete voltages or current levels caused by semiconductor crystal defects. Burst noise tends to occur in the low-frequency region.

For more details on noise → Click Here

3.14. Response times

Response times are important characteristics specified only for comparators.

Response times indicate the speed of low-to-high and high-to-low transitions of an output in response to a stepped input. Although the response times of a comparator are similar to the slew rate of an op-amp, the unit of measure for response times is time. The output of a comparator with

shorter response times responds faster to input changes. Therefore, comparators with short response times should be selected.

Low-to-high and high-to-low response times are specified for comparators. The low-to-high response time is defined as the time required for the output voltage to change from 10% to 90% of its range whereas the high-to-low response time is defined as the time required for the output voltage to change from 90% to 10% of its range. A difference between a voltage to be monitored and a reference voltage is called overdrive voltage. Generally, comparators with higher overdrive voltage provide shorter response times.

There are similar electrical characteristics called propagation delay times, which are defined as the time from an intersection of the stepped noninverting and inverting input voltage waveforms to when the output voltage reaches 50% of its maximum swing. Propagation delay times are specified for low-to-high and high-to-low input transitions.

Fig.3.14.1 shows low-to-high and high-to-low response times.

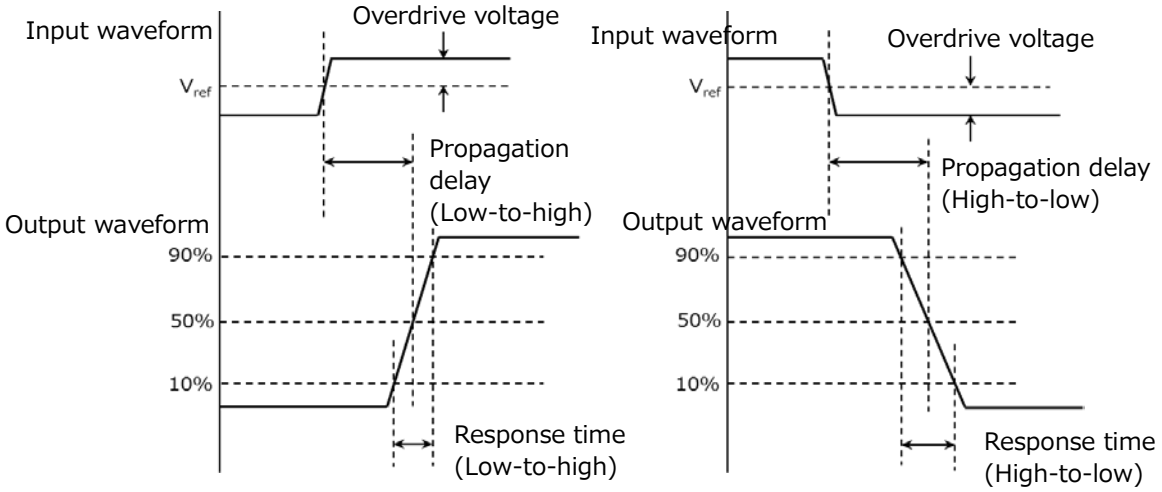


Fig.3.14.1 Response times of a comparator

4. Absolute maximum ratings

This section describes the absolute maximum ratings that must be adhered to when using op-amps and comparators.
None of the absolute maximum ratings must be exceeded during operation, even instantaneously. Exposure to a condition exceeding an absolute maximum rating can destroy a device, cause its electrical characteristics to deteriorate, or damage neighboring devices.
Great care should be exercised to ensure that none of the absolute maximum ratings is exceeded under any conditions, including supply voltage fluctuations, variations among devices, changes in the ambient temperature, and input signal fluctuations. Select op-amps and comparators with sufficient margins.

4.1. Supply voltage

Supply voltage specifies a range of voltage that can be applied across the positive and negative power supply terminals of an op-amp or a comparator.
In the case of op-amps and comparators intended for use with dual power supplies, supply voltage might be specified as ±X (V) in data sheets. In this case, the assumption is that GND is the midpoint of the positive and negative power supply voltages. Alternatively, positive and negative power supply voltages may be asymmetrical as long as their difference is lower than the maximum ratings. When operating dual-supply op-amps and comparators with a single positive using the negative power terminal as GND, up to 2X (V) can be applied to the positive power terminal.
In contrast, for op-amps and comparators intended for use with a single power, only the voltage that can be applied to the positive power terminal might be specified in data sheets, assuming that the negative power terminal is connected to GND. Such op-amps and comparators can also be used with dual power supplies. In this case, GND is the midpoint of the dual power supplies, one half of the rated voltage is applied to the positive power terminal, and minus one half of the rated voltage is applied to the negative power terminal.

4.2. Differential input voltage

Differential input voltage indicates the limit that can be applied across the noninverting and inverting input terminals. In this case, the noninverting input voltage may be higher or lower than the inverting input voltage.

4.3. Common-mode input voltage

Common-mode input voltage is the maximum difference in the voltages that can be applied to the noninverting and inverting input terminals. The common-mode input voltage shown in the Electrical Characteristics table indicates a range of voltage in which an op-amp or a comparator functions correctly whereas the common-mode input voltage shown in the Absolute Maximum Ratings table shows a range of voltage that can be applied to an op-amp or a comparator without damaging the device or causing its characteristics to deteriorate.
Common-mode input voltage must not exceed the supply voltage. In the data sheet,

common-mode input voltage is specified at a supply voltage equal to its absolute maximum rated value. It should be noted that common-mode input voltage must not exceed the absolute maximum rated supply voltage, regardless of the value specified in the data sheet.

4.4. Power dissipation

Power dissipation specifies the maximum power that can be dissipated in an IC. Normally, power dissipation is specified at an ambient temperature of 25°C. The permissible power dissipation decreases as the ambient temperature increases. Care should be taken when using an op-amp or a comparator in a high-temperature environment. Data sheets provide a derating curve showing the relationship between the ambient temperature and power dissipation. Ensure that power dissipation does not exceed this curve at the ambient temperature at which an op-amp or a comparator will be used. Fig.4.4.1 shows an example of a derating curve.

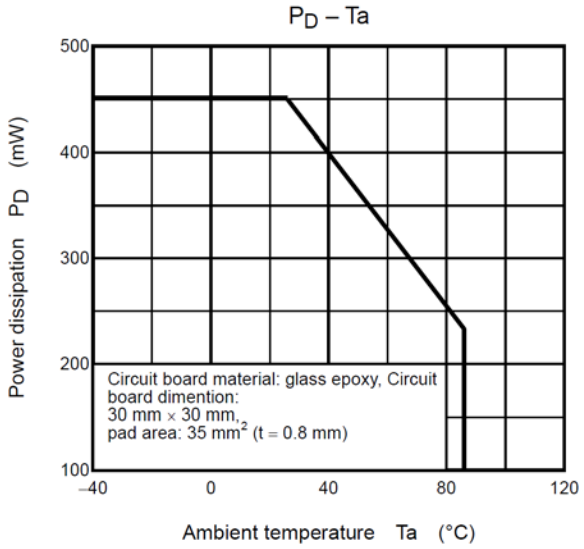


Fig.4.4.1 Example of an ambient temperature-vs-power dissipation curve (Derating curve)

In this example, an IC can dissipate up to 450 mW at an ambient temperature of 25°C and up to only roughly 230 mW at 85°C.

4.5. Operating temperature and storage temperature

Operating temperature specifies the ambient temperature range in which an IC can be used. Attach a heatsink if necessary, considering a rise in temperature due to IC heating.
Storage temperature specifies the temperature range in which an IC can be stored without causing any degradation of IC characteristics. The IC must be stored within the specified temperature range.

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